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(54) **ALUMINUM ALLOY WIRING LAYER, MANUFACTURING THEREOF, AND ALUMINUM ALLOY SPUTTERING TARGET.**

(57) An aluminum alloy wiring layer includes only scandium of 0.01-1.0 weight %, or includes scandium of 0.01-1.0 weight % and at least one kind of element of 0.1-3.0 weight % selected from the group comprising silicon, titanium, copper, boron, hafnium and rare earth elements (but scandium is excluded). The residual part of the aluminum alloy wiring layer is aluminum of 99.99 % or more in purity. This wiring layer, its manufacturing method and an aluminum alloy sputtering target used therein are suitable to large scale integrated circuits of the next generation.

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TECHNICAL FIELD

The present invention relates to an aluminum alloy wiring layer, a method of producing the same and an aluminum alloy sputtering target used for producing the same.

BACKGROUND ART

Semiconductor logic devices including a microprocessor and semiconductor memory devices represented by a DRAM are inevitable as a central processing unit, an internal memory or an external memory of a computer and the like. In the process for producing such a large-scale integrated circuit, development of wiring technique for connecting several million to several ten million semiconductor transistors in one chip with high reliability is very important.

At present, DRAM's of 16 megabits using wiring layers having a width of 0.7 to 0.8 μm and composed of an aluminum alloy material obtained by adding a small amount of silicon (Si) or a small amount of silicon and copper (Cu) to aluminum (Al), are ready for full-scale mass production.

These wiring layers are produced by forming a thin film of about 1 μm in thickness on a silicon wafer by sputtering and forming a minute wiring pattern to the thin film by lithography. In producing these wiring layers, an Al-Si alloy target containing about 1 wt.% of Si or an Al-Si-Cu alloy target containing about 1 wt.% of Si and about 0.5 wt.% of Cu is used.

With the recent development of advanced large-scale integrated circuits following DRAM's of 64 megabits and with the recent development of wiring layers having a narrower width (e.g., 0.3 to 0:6 μm) aimed at increasing the integration and the performance of semiconductor integrated circuits, a wiring technique having higher reliability has been demanded.

Al-Si alloy wiring layers or Al-Si-Cu alloy wiring layers used at present, however, have low reliability because an additive such as silicon precipitate during the manufacturing process and remains on the circuit, or breakage of wire is frequently caused thereby.

The breakage of an aluminum wire is ascribed to phenomena called electromigration and stress migration. The electromigration is a phenomenon in which metal ions are moved in wiring in accordance with an electric field by electric currents in the wiring and this effect causes voids on the grain boundary, thereby breakaging the wire. The stress migration is a phenomenon of breakage of wire caused by which the tensile stress is produced on the aluminum wire in accordance with the difference in the thermal expansion between the aluminum wire and the barrier film of SiN or the like laminated, thereby producing voids on the grain boundary.

DISCLOSURE OF THE INVENTION

As a result of studies undertaken by the present inventors so as to solve the above-described problems in the prior art, and to provide a wiring layer which scarcely causes breakage of wire and which has a low electrical resistance, the following has been found.

Scandium (Sc) combines with Al to form a minute intermetallic compound ($ScAl_3$), which disperses in Al, thereby producing a wire breakage preventing effect. $ScAl_3$ is different from the intermetallic compound $CuAl_2$ which is formed by combining Cu with Al, thereby not becoming coarse by the the heat treatment (400 to 450 °C) which is inevitable after the formation of a thin film.

The heat treatment herein means to an anealing treatment carried out for the purpose of making stable a metal thin film from the amorphous thin film and enhancing the adhesiveness thereof.

The present invention has been achieved on the basis of this finding.

In a first aspect of the present invention, there is provided an aluminum alloy wiring layer comprising 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%.

In a second aspect of the present invention, there is provided an aluminum alloy wiring layer comprising 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium and the balance aluminum having a purity of not less than 99.99%.

In a third aspect of the present invention, there is provided an aluminum alloy sputtering target comprising 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%.

In a fourth aspect of the present invention, there is provided an aluminum alloy sputtering target comprising 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium and the

balance aluminum having a purity of not less than 99.99%.

In a fifth aspect of the present invention, there is provided a process for producing an aluminum alloy wiring layer comprising sputtering an aluminum alloy target composed of 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99% or an aluminum alloy target composed of 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium, and the balance aluminum having a purity of not less than 99.99%.

The present invention will be explained in detail hereinunder.

In an aluminum alloy sputtering target of the present invention, a high-purity aluminum having a purity of not less than 99.99% is used as a base metal. Such a high-purity aluminum can be obtained by electrolytic refining, fractional crystallization, fractional distillation, crystallization or the like.

In the present invention, 0.01 to 1.0 wt.% of scandium, or 0.01 to 1.0 wt.% of scandium and 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium is added to such a high-purity aluminum.

As the rare-earth elements, yttrium, lanthanum, cerium, praseodymium, neodymium, promethyum, samarium, europium, gadolinium and terbium may be exemplified. If the amounts of scandium contained therein and the amount of specific element contained together with scandium are out of the above-described ranges, the object of the present invention does not become to be attained. The particularly preferred scandium content is in the range of 0.05 to 0.6 wt.%.

In the present invention, the aluminum alloy is produced by adding a predetermined amount of scandium, or scandium and specific element to a high-purity aluminum, casting the resultant mixture to obtain an ingot containing not more than 10 ppm of inevitable impurities, and applying the ingot to a heat-treatment, rolling-treatment, and reheat-treatment in order so as to form a material having uniform fine crystals.

The conditions for the respective treatments are not specified, but heat-treatment is generally carried out at 500 to 550 °C for 10 to 15 hours, rolling-treatment is generally carried out at a reduction ratio of 50 to 90%, and reheat-treatment is generally carried out at 400 to 450 °C for 30 to 60 minutes.

The aluminum alloy material obtained in this way is cut into a shape (e.g., circle, rectangle, and doughnut-like shape in which the central part of the above-mentioned shapes is bored) in accordance with a sputtering apparatus, thereby producing a sputtering target.

An aluminum alloy wiring layer according to the present invention is produced by sputtering using the thus-obtained aluminum aloy sputtering target comprising 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%, or an aluminum alloy target comprising 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium and the balance aluminum having a purity of not less than 99.99%. The known sputtering apparatus and sputtering conditions may be adopted for the sputtering.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graph showing the measured resistivities of the thin films obtained in Example and Comparative Example, wherein the ordinate represents a resistivity ($\mu\Omega$m) and the abscissa represents a wafer temperature (°C); the curves (1) to (4) show the samples 1 to 4, respectively, in Example, and (11) and (12) show the samples 11 and 12 respectively in Comparative Example (the same in Figs. 2 and 3).

Fig. 2 is a graph showing the results of the electromigration test of the thin films obtained in Example and Comparative Example, wherein the ordinate represents a disconnection time (hour) and the abscissa represents a wafer temperature (°C).

Fig. 3 is a graph showing the results of the stress migration test of the thin films obtained in Example and Comparative Example, wherein the ordinate represents the number of voids and the abscissa represents a wafer temperature (°C).

Fig. 4 is an explanatory view of the entire part of the wiring pattern for the electromigration test.

Fig. 5 is an enlarged explanatory view of the main part of the wiring pattern for the electromigration test shown in Fig. 4.

Fig. 6 is an explanatory view of the wiring pattern for the stress migration test.

Fig. 7 is an explanatory view of the wiring pattern for the stress migration test.

Fig. 8 is an explanatory view of a heating plate used for the stress migration test.

In Figs. 7 and 8, the symbol B represents a wedge-shaped void, and the reference numeral 1 represents a heating plate, the reference numeral 2 represents a presser plate, the reference numeral 3

represents a heater and the reference numeral 4 represents a wafer.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will be explained in more detail with reference to the following example, but it is to be understood that the present invention is not restricted thereto.

The measurement of electrical resistance, the electromigration test and the stress migration test in the following example and comparative example were carried out by the following methods.

(Measurement of electrical resistance)

The sheet resistance was measured by an ohmmeter, and after a part of the thin film is dissolved and removed by etching, the thickness of the thin film was measured by a micro step hight meter. The resistivity was obtained from the follow-ing formula, and this was expressed as the electrical resistance.

Resistivity = (sheet resistance)x(thickness of the thin film)

(Electromigration test)

A wafer with a wiring pattern formed thereon was brought into close contact with a heating plate and heated to 200 °C. Electrodes were connected between wiring patterns (1) and (2) shown in Figs. 4 and 5. An ohmmeter was con-nected between (3) and (4). Disconnection was detected applying a direct current having a current density of 2×10^7 A/cm^2 between the electrodes, and the time elapsed until the disconnection was measured.

Fig. 4 is an explanatory view of the entire wiring pattern for the electromigration test, and Fig. 5 is an enlarged explanatory view of the main part of the wiring pattern shown in Fig. 4.

(Stress migration test)

A wafer (4) with a wiring pattern formed thereon was brought into close contact with a heating plate (1) shown in Fig. 1 having a convex central portion protruding from the peripheral portion by 0.2 mm, so that the wafer (4) was curved and a tensile stress was applied to the wire. Thereafter, the wafer (4) was heated at 400 °C for 5 minutes, and the number of voids produced at the portion represented by the wiring pattern (E) in Fig. 6 was counted. Only the number of voids (B) produced in the shape of a wedge on the side surfaces of the wiring layer and having a length of not less than 1 µm was measured.

Fig. 8 is an explanatory view of a heating plate used for the stress migration test. In Fig. 8, the reference numeral 1 represents a heating plate, the reference numeral 2 represents a presser plate, the reference numeral 3 represents a heater and the reference numeral 4 represents a wafer, and the symbol B represents a wedge-shaped void.

Example and Comparative Example

A predetermined amount of metal element shown in Table 1 was added to a refined high-purity aluminum having a purity of not less than 99.999%, and the molten material was cast.

The ingot obtained was heat-treated at 525 °C for 12 hours, rolled at a reduction ratio of 70%, and then reheated at 425 °C for 45 minutes, thereby obtaining a material having uniform fine crystals.

The material obtained was machined to produce a discal sputtering target 250 mm in diameter and 15 mm in thickness.

Each sputtering target was mounted on a magnetron sputtering apparatus MLX-3000 (produced by Ulvac Corp.) and a thin film of 1 µm in thickness was formed on the surface of a silicon wafer 6 inches in diameter with an SiO_2 thin film having 0.2 µm in thickness formed thereon. Thereafter, the silicon wafer was heat-treated at 450 °C for 15 minutes by lamp heating. The magnetron sputtering apparatus was operated under the following conditions.

Base pressure degree of vacuum : 6×10^{-8} torr

Ar pressure : 4×10^{-3} torr

Sputtering electric power: 5 Kw

Wafer heating temperature: 150 °C, 200 °C, 250 °C

These wafer heating temperatures were the condition adopted for carrying out an acceleration test.

Each thin film obtained was subjected to the measurement of the electrical resistance, an electromigration test and a stress migration test.

The results are shown in Figs. 1 to 3.

Fig. 1 is a graph showing the measured electrical resistances, Fig. 2 is a graph showing the results of the electromigration test, and Fig. 3 is a graph showing the results of the stress migration test. In these drawings, the curves (1) to (4) and (11) and (12) correspond to the sample numbers in Table 1.

The results of the measurement of the electrical resistances, the electromigration test and the stress migration test at a wafer heating temperature of 200 °C are shown in Table 1.

Table 1

	Added Element (wt.%)								Resistivity	EM Test*1	SM Test*2
	Sc	Cu	Si	Ti	B	Hf	Y	Ce	(μΩcm)	(Hours)	(Number)
EXAMPLE											
Sample 1	0.05	--	--	--	--	--	--	--	2.78	38.0	16
Sample 2	0.10	--	--	--	--	--	--	--	2.73	77.6	13
Sample 3	0.20	--	--	--	--	--	--	--	2.73	107.8	5
Sample 4	0.20	0.50	--	--	--	--	--	--	2.88	119.5	3
Sample 5	0.20	--	1.00	--	--	--	--	--	2.74	110.0	3
Sample 6	0.10	--	--	0.02	--	--	--	--	2.80	89.3	6
Sample 7	0.10	--	--	--	0.03	--	--	--	2.75	81.7	10
Sample 8	0.10	--	--	--	--	0.02	--	--	2.82	90.0	5
Sample 9	0.10	--	--	--	--	--	0.05	--	2.88	97.8	8
Sample 10	0.10	--	--	--	--	--	--	0.05	2.96	90.6	12
COMPARATIVE EXAMPLE											
Sample 11	--	--	1.00	--	--	--	--	--	3.08	10.0	40
Sample 12	--	0.50	1.00	--	--	--	--	--	3.23	31.7	22
Sample 13	--	--	--	--	--	--	0.20	--	3.05	33.4	30
Sample 14	--	--	--	--	--	--	--	0.20	3.10	20.0	32
Sample 15	2.00	--	--	--	--	--	--	--	3.31	30.3	5

(Note)
*1: Electro migration Test (Time elapsed until disconnection)
*2: Stress migration Test (Number of voids)

INDUSTRIAL APPLICABILITY

The aluminum alloy sputtering target according to the present invention has a low resistivity and takes a long time until disconnection generates. In addition, the number of voids produced is small. Thus, it is excellent as a wiring material. The wiring layer using the aluminum alloy sputtering target according to the

present invention has a great resistance to electromigration and stress migration, and has a high reliability, so that it is suitable as a wiring layer for an advanced large-scale integrated circuit.

Claims

1. An aluminum alloy wiring layer comprising 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%.

2. An aluminum alloy wiring layer comprising 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium, and the balance aluminum having a purity of not less than 99.99%.

3. An aluminum alloy wiring layer according to any one of Claims 1 and 2, wherein the scandium content is 0.05 to 0.6 wt.%.

4. A process for producing an aluminum alloy wiring layer comprising sputtering an aluminum alloy target composed of 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%

5. A process for producing an aluminum alloy wiring layer comprising sputtering an aluminum alloy target composed of 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium, and the balance aluminum having a purity of not less than 99.99%.

6. A process for producing an aluminum alloy wiring layer according to any one of Claims 4 and 5, wherein the scandium content in said aluminum alloy target is 0.05 to 0.6 wt.%.

7. An aluminum alloy sputtering target comprising 0.01 to 1.0 wt.% of scandium and the balance aluminum having a purity of not less than 99.99%.

8. An aluminum alloy sputtering target comprising 0.01 to 1.0 wt.% of scandium, 0.01 to 3.0 wt.% of at least one element selected from the group consisting of silicon, titanium, copper, boron, hafnium and rare-earth elements other than scandium, and the balance aluminum having a purity of not less than 99.99%.

9. An aluminum alloy sputtering target according to any one of Claims 7 and 8, wherein the scandium content is 0.05 to 0.6 wt.%.

FIG. 1

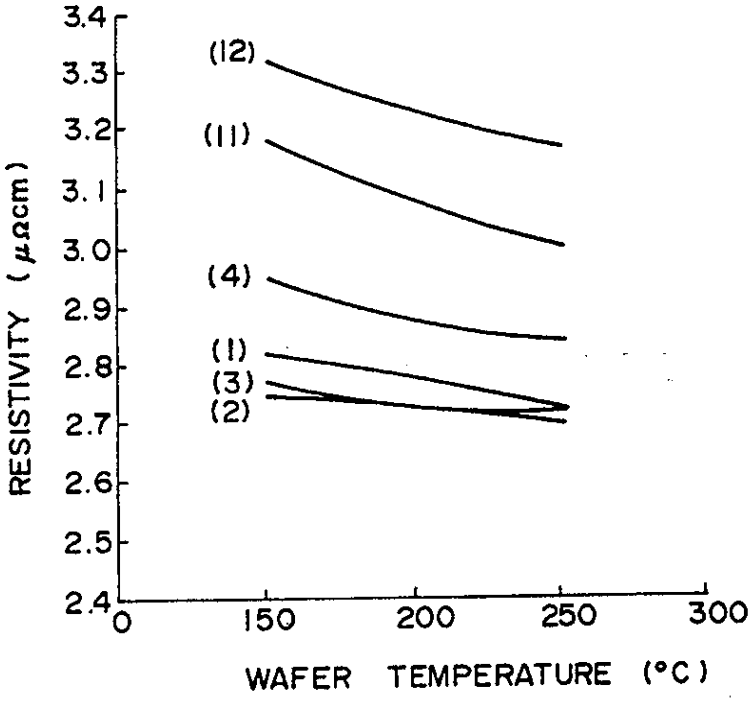

RESISTIVITY (μΩcm)
3.4
3.3
3.2
3.1
3.0
2.9
2.8
2.7
2.6
2.5
2.4
(12)
(11)
(4)
(1)
(3)
(2)
0
150
200
250
300
WAFER TEMPERATURE (°C)

FIG. 2

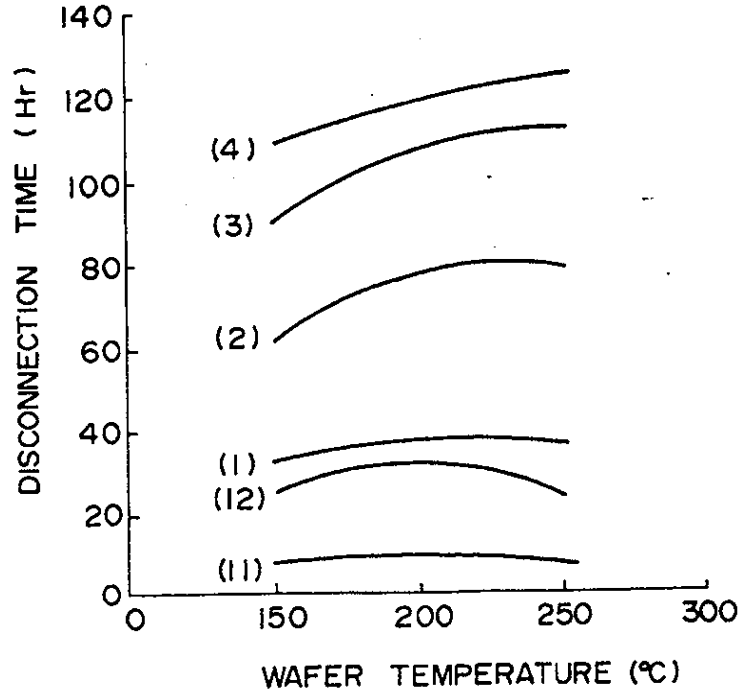

DISCONNECTION TIME (Hr)
140
120
100
80
60
40
20
0
(4)
(3)
(2)
(1)
(12)
(11)
0
150
200
250
300
WAFER TEMPERATURE (°C)

FIG. 3

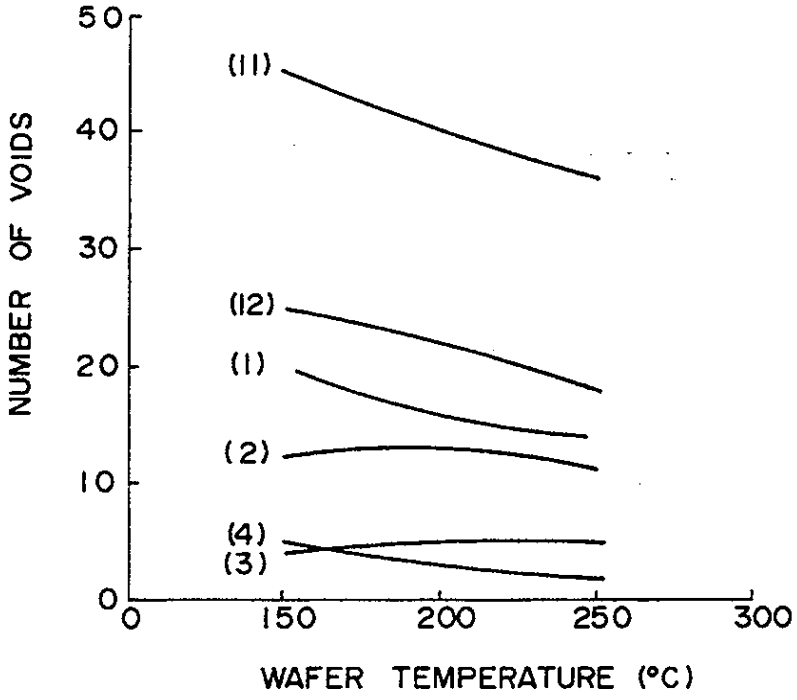

50
40
30
20
10
0
NUMBER OF VOIDS
(11)
(12)
(1)
(2)
(4)
(3)
0
150
200
250
300
WAFER TEMPERATURE (°C)

FIG. 4

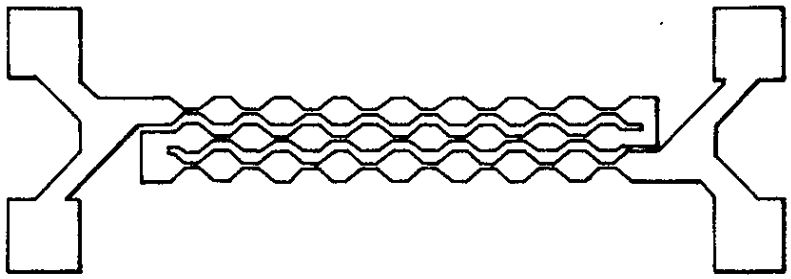


FIG. 5

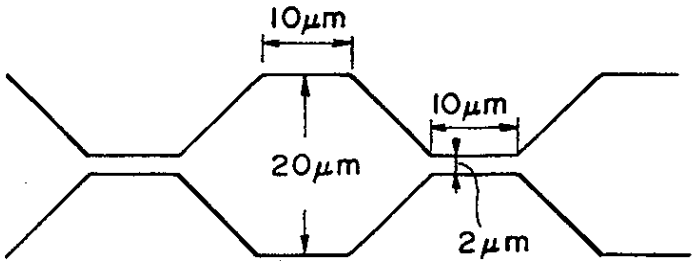


FIG. 6

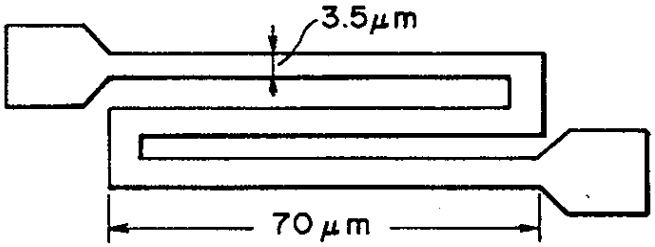


FIG. 7

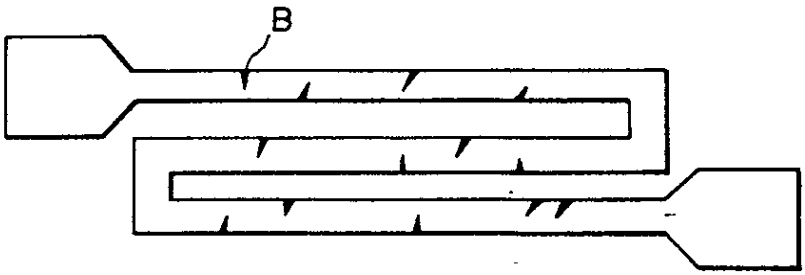
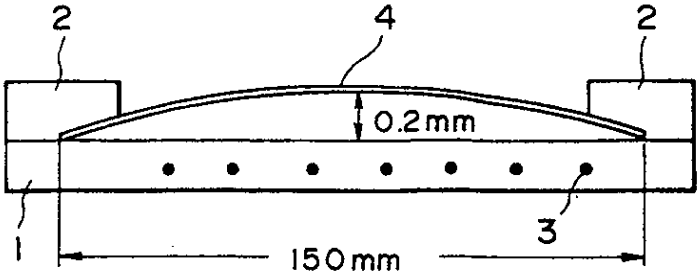


FIG. 8



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP92/00034

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H01L21/3205, C23C14/16

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H01L21/3205, C23C14/16

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho 1926 - 1991
Kokai Jitsuyo Shinan Koho 1971 - 1991

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	JP, A, 1-289140 (Nippon Telegraph & Telephone Corp.), November 21, 1989 (21. 11. 89), (Family: none)	1-9

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
April 1, 1992 (01. 04. 92)	April 21, 1992 (21. 04. 92)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	